

### REMARKS

With claims 1-19 pending, claim 11 has been cancelled with this amendment. Further claim 9 has been amended as indicated in detail below.

#### Section 102 Rejection Base on Jigour

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Jigour (U.S. Patent No. 5,991,194). The Office Action states that Jigour discloses a system comprising a serial flash memory; and a programmable logic device (PLD) having an interface coupled to the serial flash memory, wherein the interface is configured to identify the serial flash memory. The Office Action cites Jigour, col. 3, lines 59-61 stating that the flash memory array 124 is fully accessible through a four-pin serial peripheral interface. This rejection is respectfully traversed.

In contrast with the Office Action, Jigour does not disclose a PLD as claimed in claims 1-3. Jigour does not identify any particular device that communicates with a serial flash memory. Applicant's disclosure paragraphs [0002]-[0004] and [0017] indicates that a typical PLD is not configured for recognition of multiple serial flash memories for communication. Accordingly, claims 1-3 are not believed anticipated by Jigour.

#### Section 102 Rejection Base on DeCaro

Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by DeCaro (U.S. Patent No. 7,032,039). The Office Action states that DeCaro discloses a system comprising a serial flash memory; and a PLD having an interface coupled to the serial flash memory, wherein the interface is configured to identify the serial flash memory. The Office Action cites DeCaro, col. 2, lines 36-39 and col. 2, lines 45-54. This rejection is respectfully traversed.

In contrast with the Office Action, DeCaro does not disclose a PLD. DeCaro only discloses use of a microprocessor to communicate with the serial flash memory device. Accordingly, claims 1-3 are believed not anticipated by DeCaro.

Section 103 Rejection

Claims 4-9, 11 and 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jigour or DeCaro in view of a well known feature in the art of which official notice is taken. Based on the above amendments and the following remarks, this rejection is believed to be overcome.

Initially, Applicant notes that reference to claim 11 as rejected appears to be a mistake, with claim 12 instead believed intended for this rejection. The cover page of the Office Action reflects the mistake, indicating claim 12 is rejected, while claim 11 is only objectionable. Further, in paragraph 6, claim 11 is indicated as allowable subject matter once objections are overcome, while claim 12 is not. This response will proceed assuming that claim 12 is covered under the Section 103 rejection, while claim 11 is not.

Regarding claims 4-8, the Office Action states that Jigour or DeCaro discloses the claimed invention, but fails to specifically disclose an address register to provide a start address to the serial flash memory, wherein the start address identifies an initial address to be accessed in the serial flash memory. The Office Action further states that such a start address register is well known, citing patents 6,510,090, 6,549,482 and 6,829,727 for reference.

In response, initially claims 4-8 are believed allowable based at least on their dependency on claim 1. Claim 8 further claims that the PLD is an FPGA. Neither Jigour nor DeCaro disclose either a PLD, as discussed previously in this response, or a more specific type of PLD, the FPGA as claimed. Accordingly, claims 4-8 are all believed allowable as not anticipated by Jigour or DeCaro in light of other prior art.

Regarding claims 9, 12 (11 is noted in the Office Action, but 12 is believed intended to be rejected as indicated above) and 17-19, the Office action indicates that they encompass the same scope of invention as those of claims 4-8, and are similarly believed non-obvious.

In response, claim 9 has been amended to include the elements of claim 11. Accordingly, claim 11 has been cancelled. As indicated in paragraph 6 of the Office Action, claim 11 is believed allowable in independent form. Accordingly, with claim 9 including the elements of claim 11, claim 9 is believed in condition for allowance.

Claims 17-18 are believed allowable based at least on their dependency on claim 9.

Regarding claim 19, it claims "sequentially issuing a plurality of different read commands...; determining which read command causes the serial memory to respond; and identifying the serial memory from the read command that results in a response." Neither Jigour nor DeCaro disclose providing more than one read command to determine if a memory responds to enable identifying the memory. In fact, DeCaro specifically teaches away from such a structure, specifically stating that only one command is needed to contact the memory. See the DeCaro abstract stating, "The identification process, issuing the command, receiving the reply, is completed in one operation." Accordingly, claims 4-8 are all believed allowable as not patentable under 35 U.S.C. § 103 over Jigour or DeCaro in light of other prior art.

#### Allowable Subject Matter

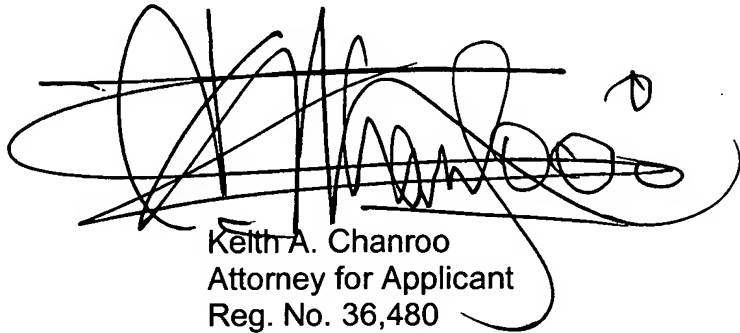
Claims 10-11 and 13-16 are objected to as being dependent upon a rejected base claim, but are indicated as being allowable if rewritten in independent form. As indicated previously, claim 9 has been amended to include the elements of claim 11 and is now believed allowable. Claims 10 and 13-16 are believed allowable based at least on their dependency on claim 9.

CONCLUSION

All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, Applicant's attorney can be reached at Tel: 408-879-7710.

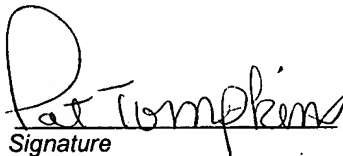
Respectfully submitted,



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*I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 22, 2006.*

Pat Tompkins  
Name



Signature